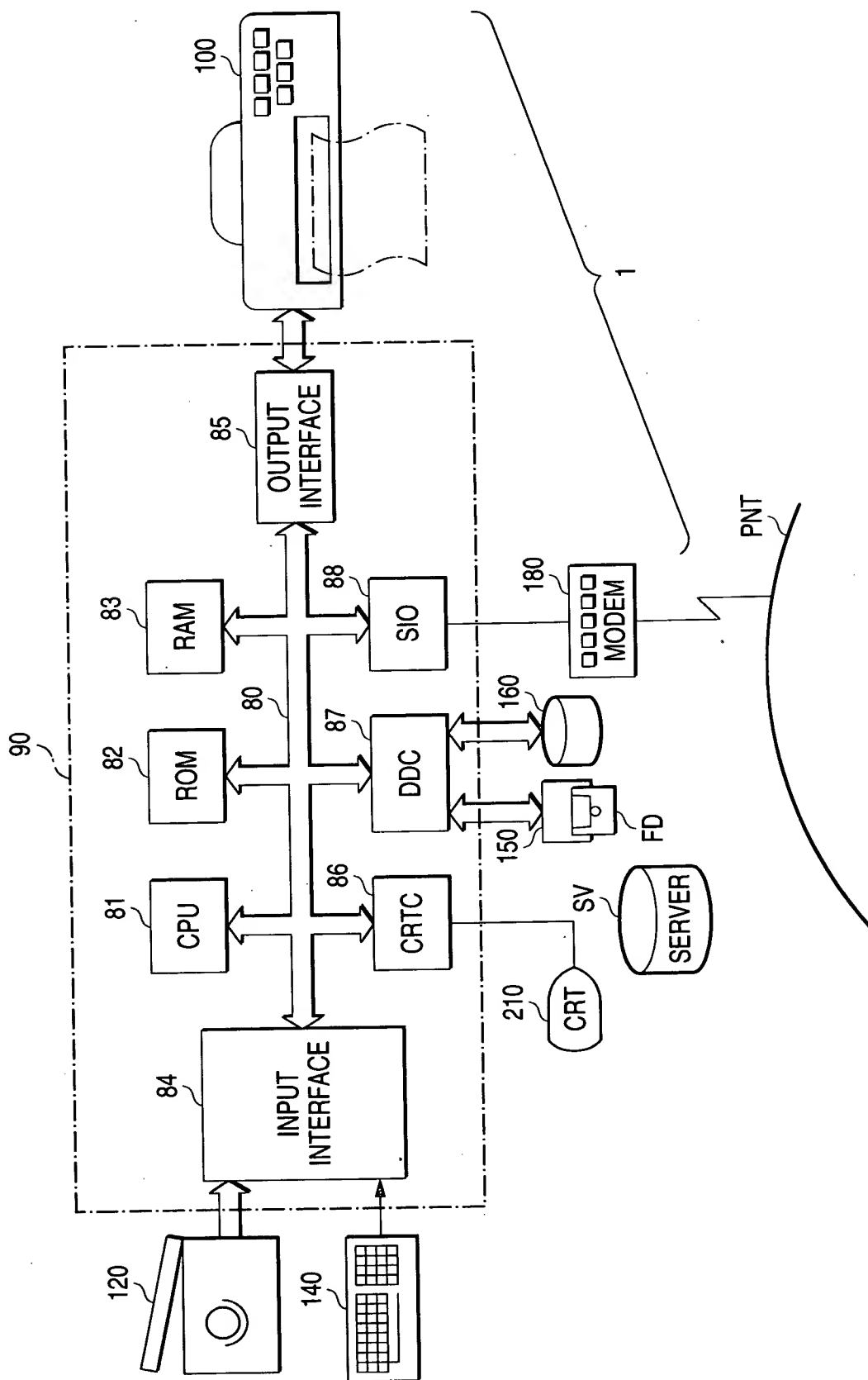


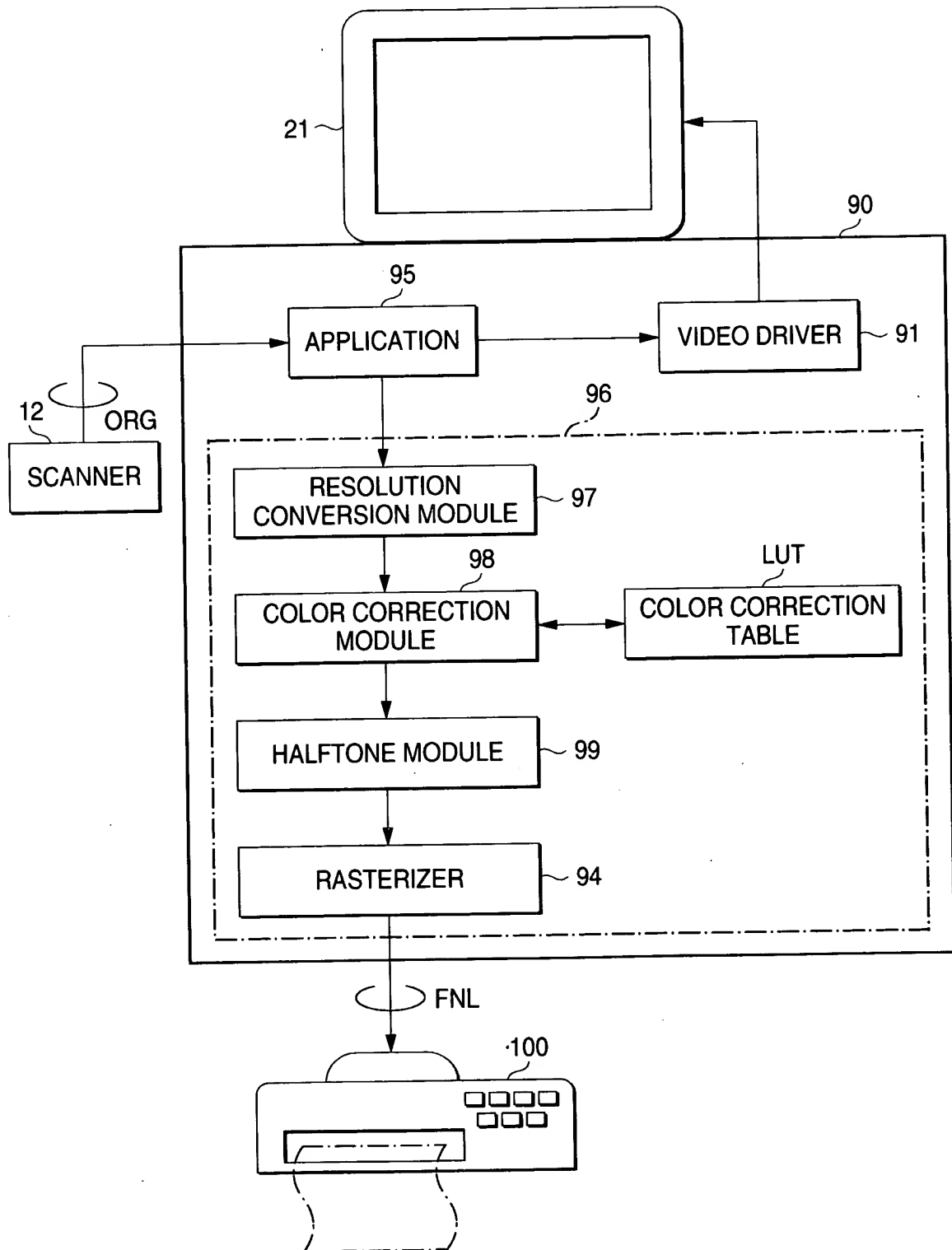
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FIG. 1



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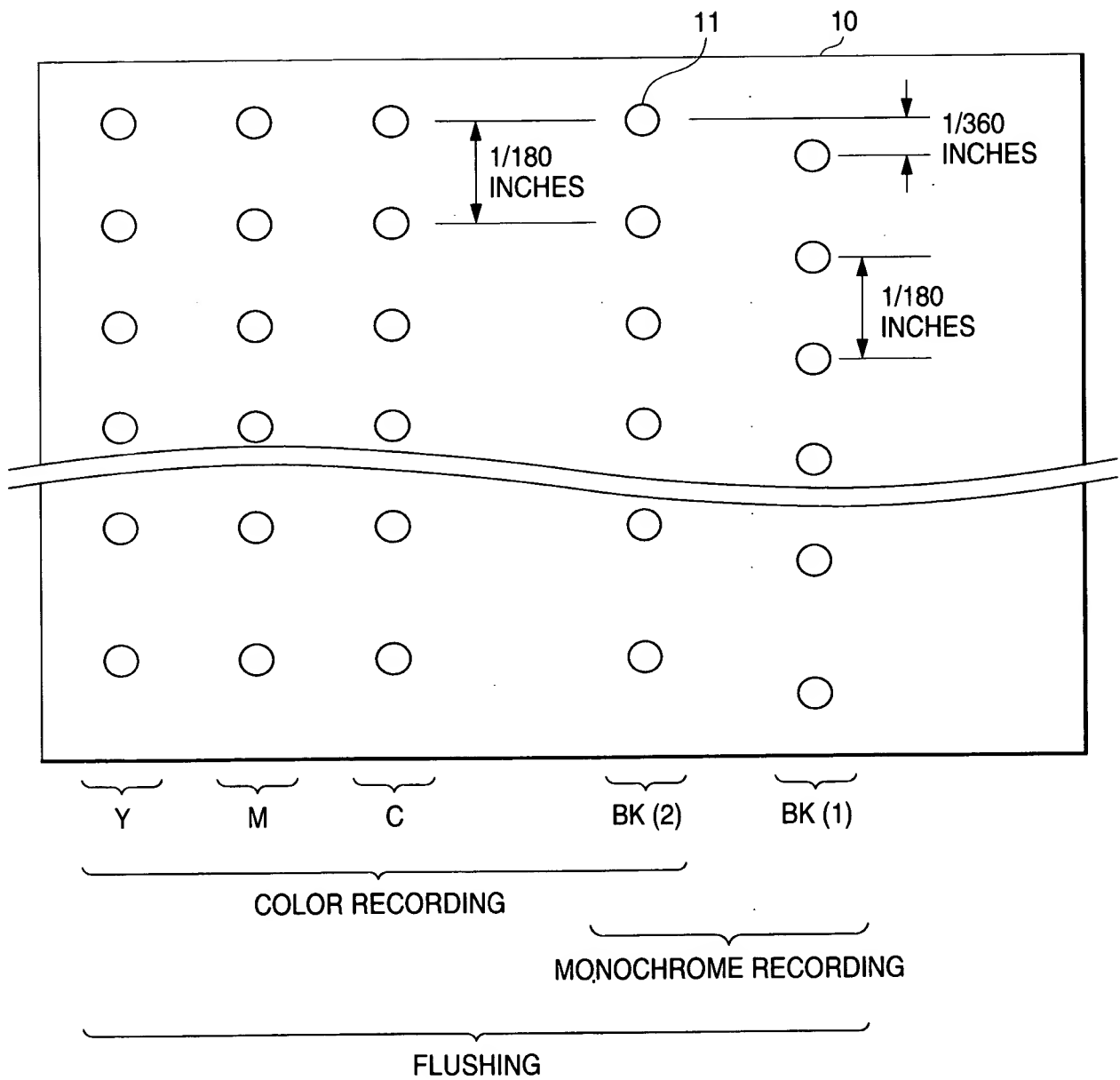
FIG. 2



[illegible]

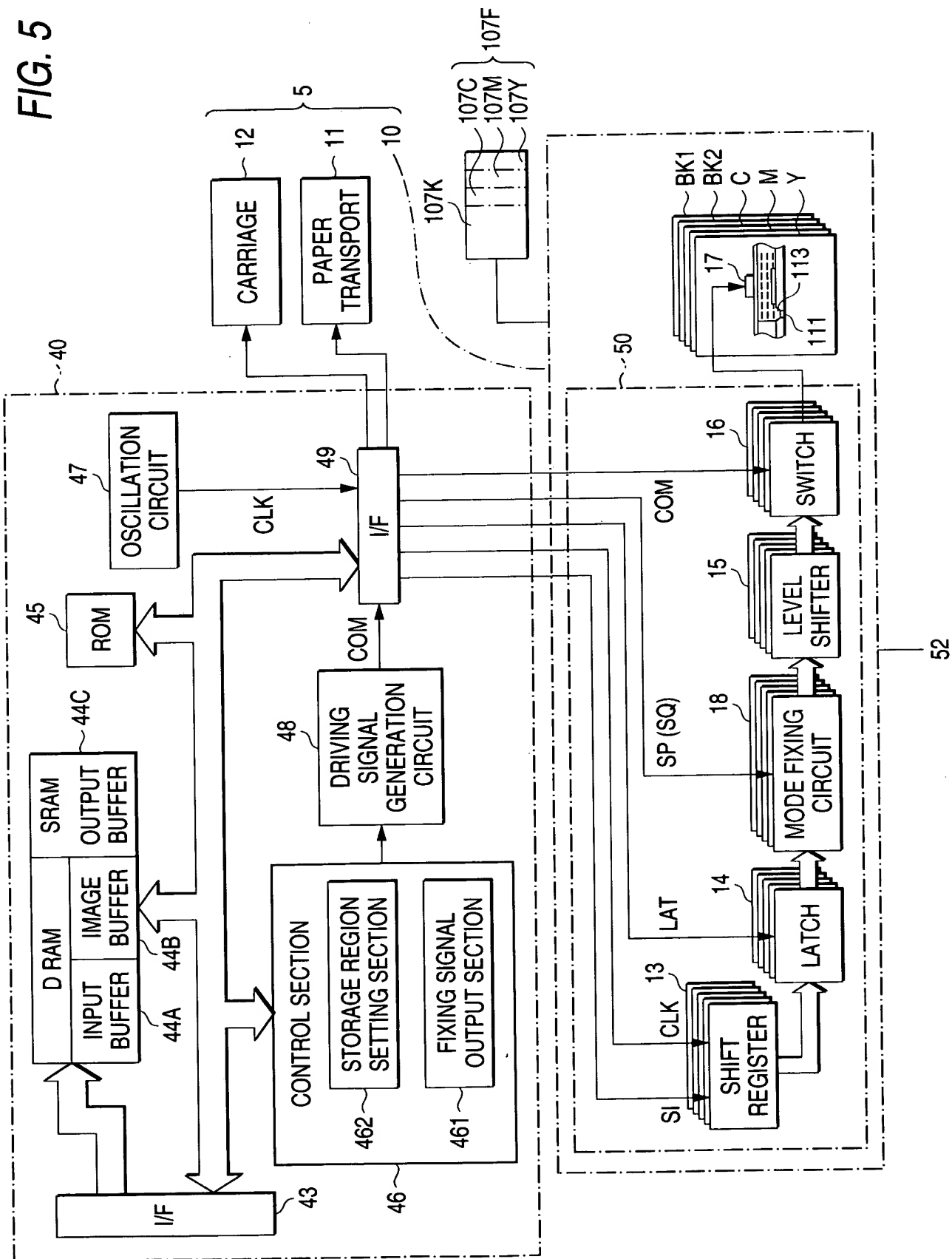
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FIG. 4



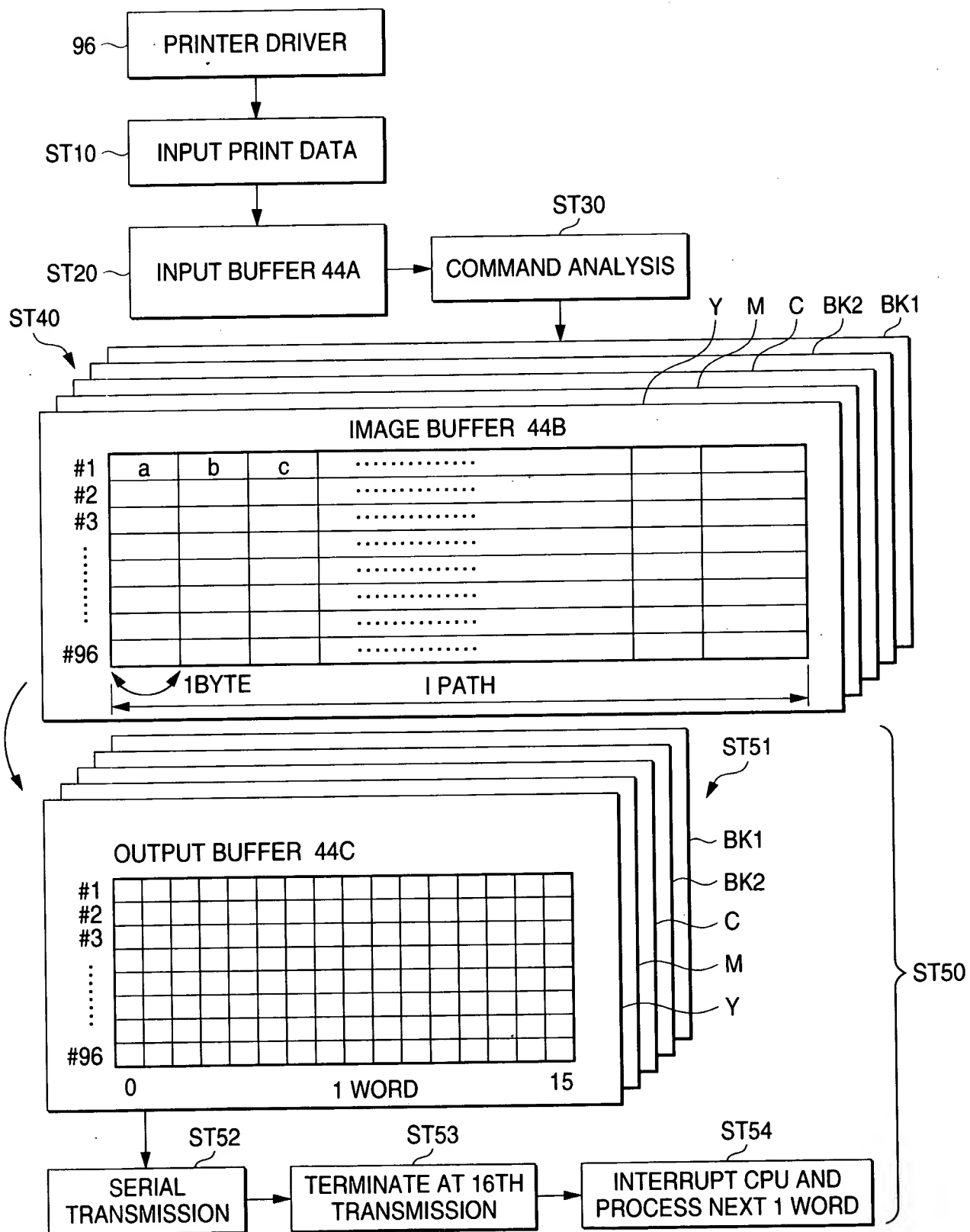
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FIG. 5



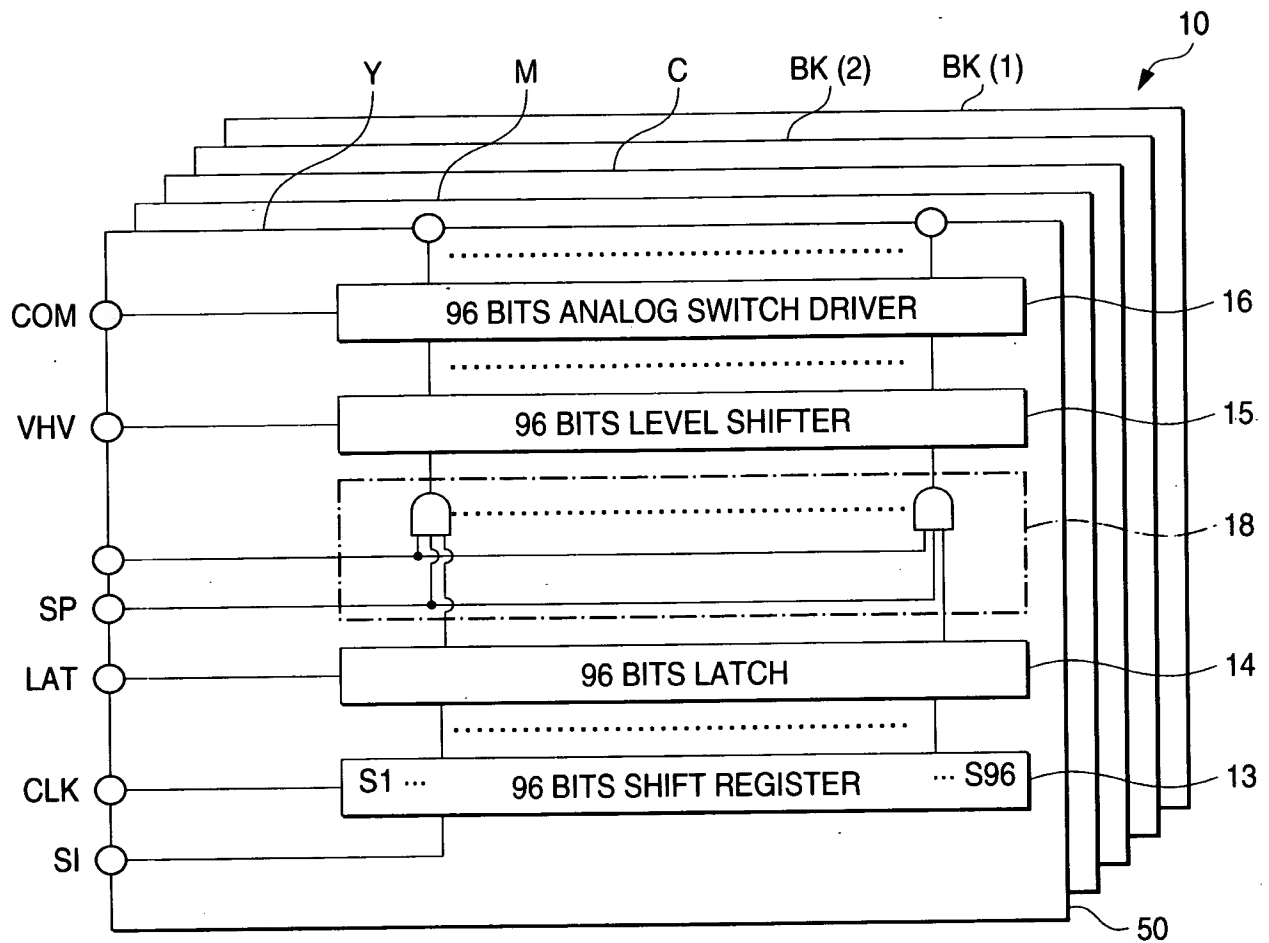
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FIG. 6



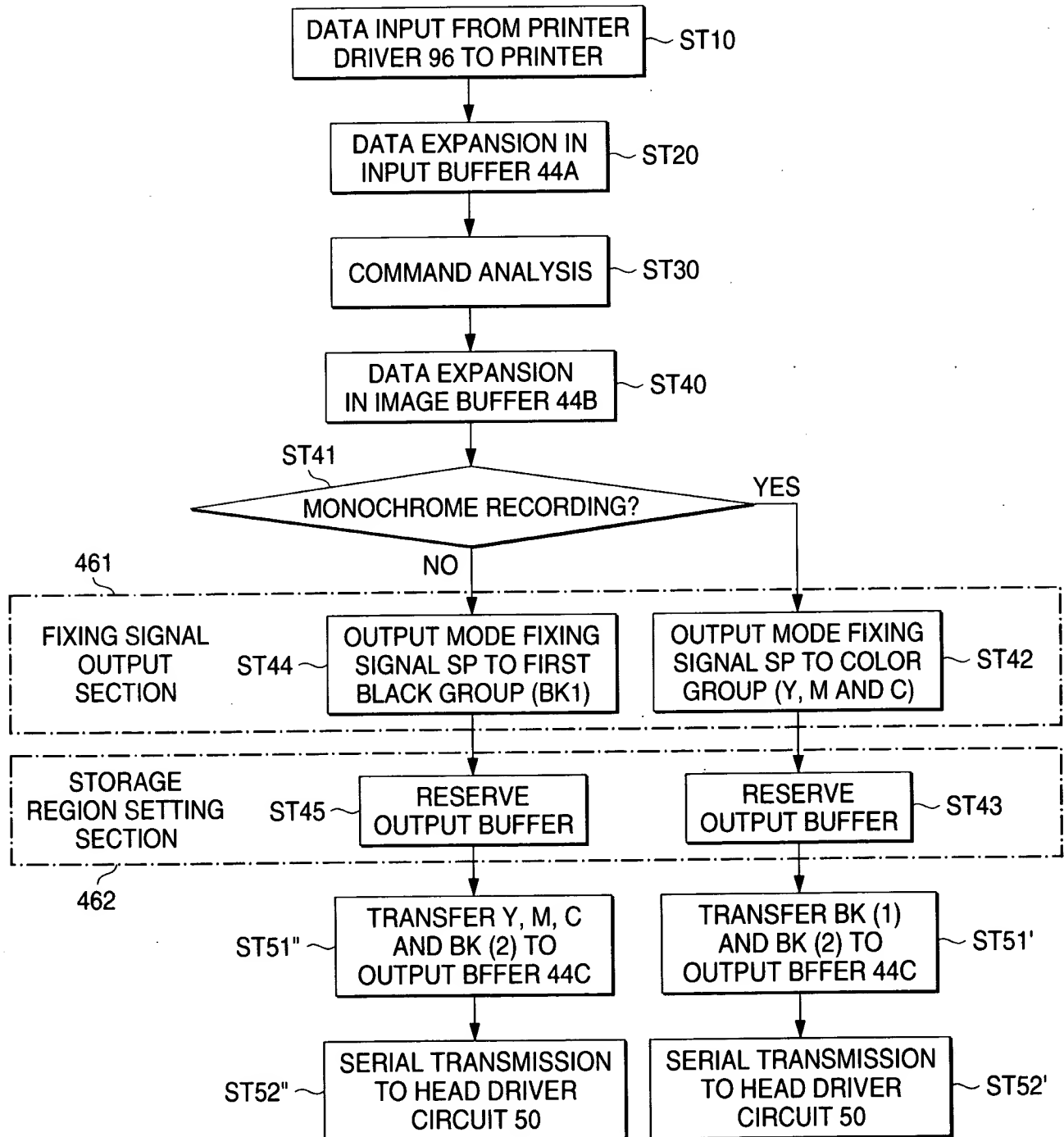
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FIG. 7



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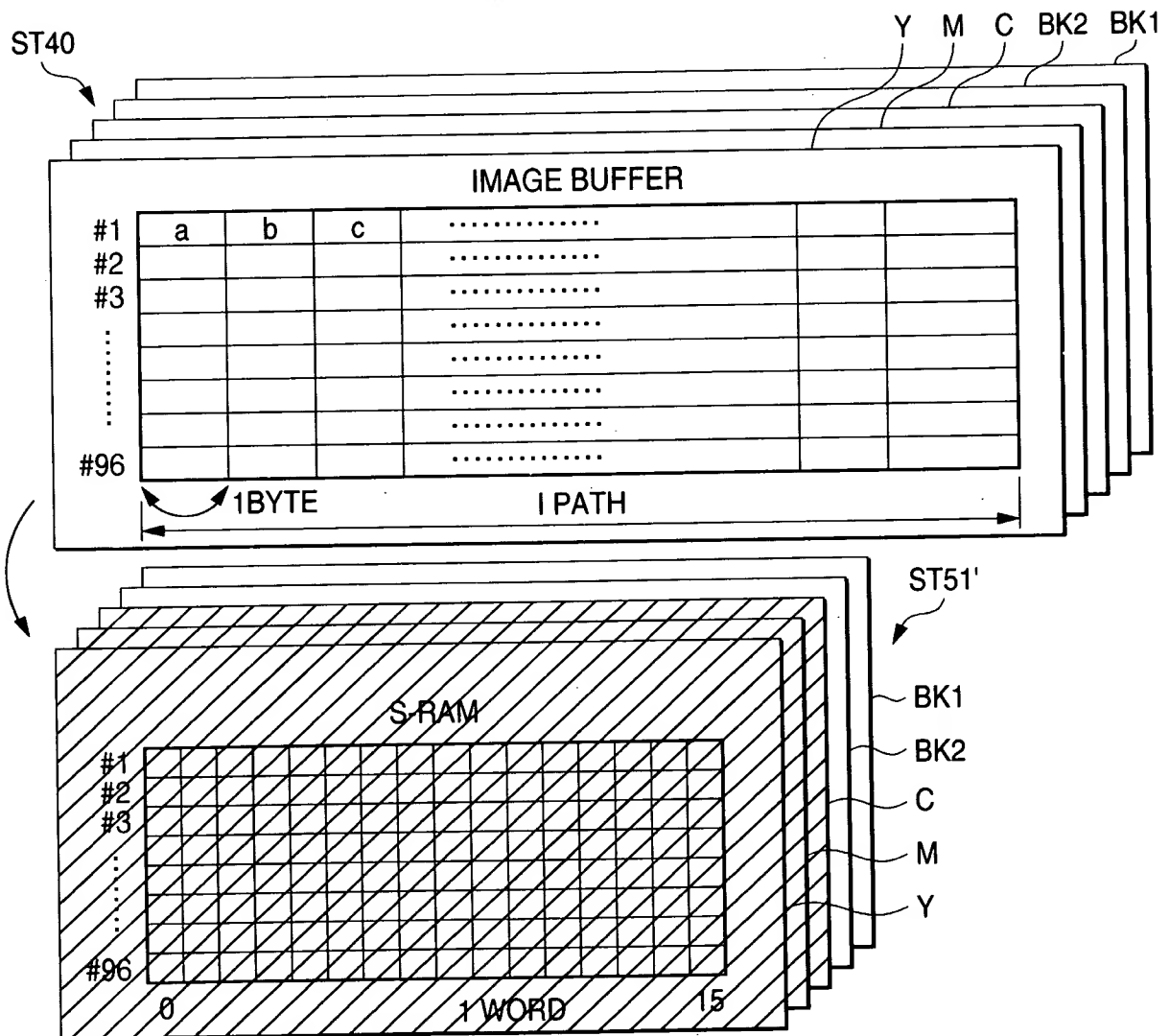
FIG. 8





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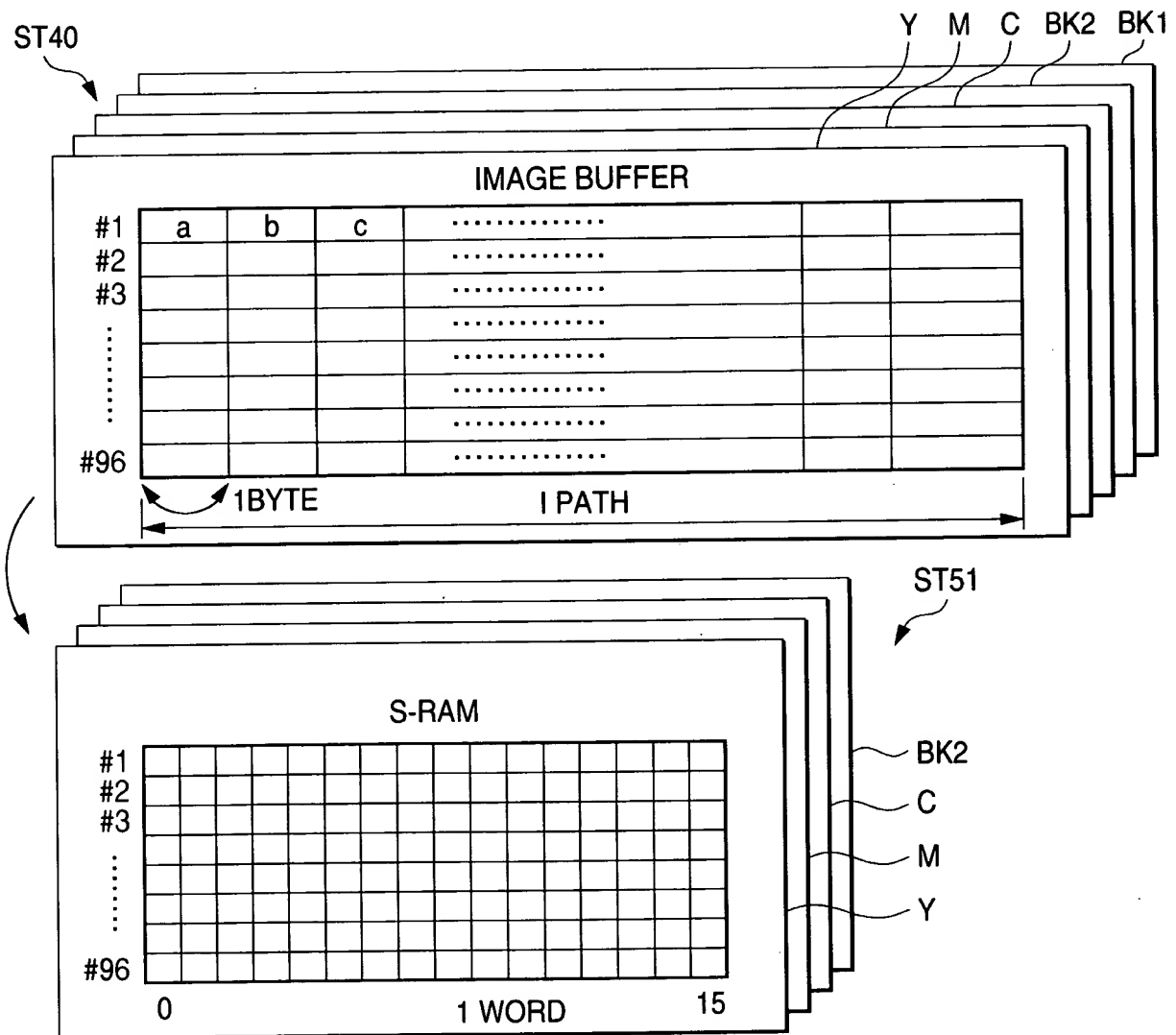
FIG. 9



The diagram illustrates the system architecture. At the top, a stack of image buffers is labeled ST40. The top buffer is detailed as an 'IMAGE BUFFER' with rows #1 to #96. Each row contains a sequence of data: 'a', 'b', 'c', followed by a dotted line, and then two empty columns. A double-headed arrow below the first three columns is labeled '1 BYTE'. A long arrow below the entire row is labeled 'I PATH'. To the right of the buffers, a stack of color planes is shown, labeled Y, M, C, BK2, and BK1 from top to bottom. An arrow points from the ST40 buffers to a stack of S-RAM units at the bottom, labeled ST51. The top S-RAM unit is detailed as an 'S-RAM' with rows #1 to #96 and columns 0 to 15. A double-headed arrow below the columns is labeled '1 WORD'. To the right of the S-RAM units, a stack of color planes is shown, labeled BK1, BK2, C, M, and Y from top to bottom.

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FIG. 11



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FIG. 12

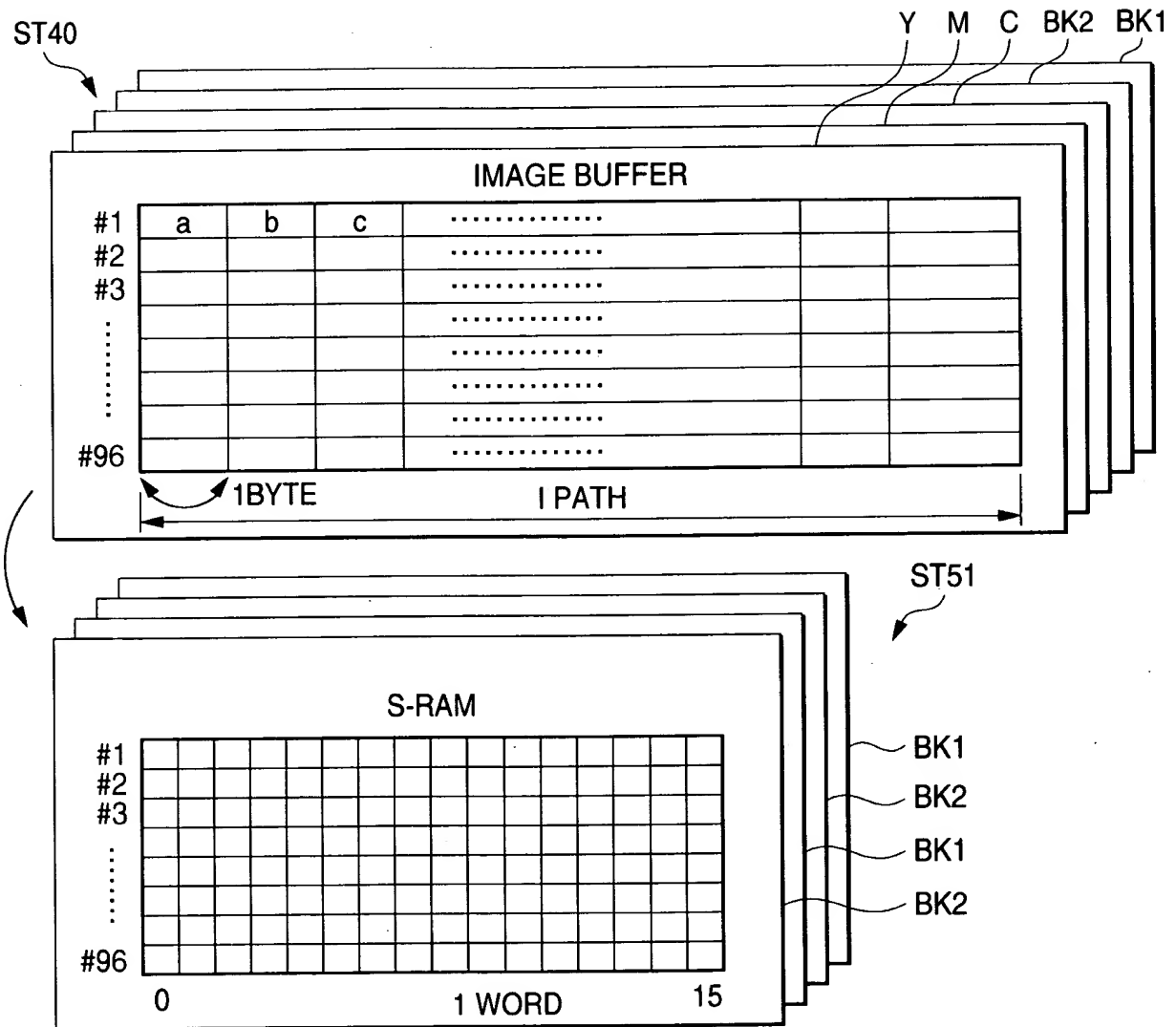


FIG. 13

